



UNITED STATES PATENT AND TRADEMARK OFFICE

14A

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/658,732	09/11/2000	Makoto Inai	P/1071-1118	4527

7590 03/17/2005
KEATING & BENNETT, LLP
10400 EATON PLACE
SUITE 312
FAIRFAX, VA 22030

EXAMINER

BROCK II, PAUL E

ART UNIT	PAPER NUMBER
----------	--------------

2815

DATE MAILED: 03/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Art Unit: 2815



UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 09/658,732
Filing Date: September 11, 2000
Appellant(s): INAI ET AL.

Peter M. Medley
For Appellant

EXAMINER'S ANSWER

MAILED

MAR 17 2005

GROUP 2800

Art Unit: 2815

This is in response to the appeal brief filed December 15, 2004 appealing from the Office action mailed May 18, 2004.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

The following is a listing of the evidence (e.g., patents, publications, Official Notice, and admitted prior art) relied upon in the rejection of claims under appeal.

Sawada et al., "A Super Low-Noise AlGaAs/InGaAs/GaAs DC-HFET with 0.15 micron Gate-Length", Japanese Journal of Applied Physics, Supplements, Extended Abstracts of the 1991 International Conference on Solid State Devices and Materials (SSDM '91), Yokohama, Japan, August 27-29, 1991, pages 353-355.

Enoki, "Delay Time Analysis for 0.4- to 5-micron-Gate InAlAs-InGaAs HEMT's" IEEE Electron Device Letters 11 (1990) November, No. 11, pp. 502-504.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-10 and 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sawada et al., "A Super Low-Noise AlGaAs/InGaAs/GaAs DC-HFET with 0.15 micron Gate-Length," (Sawada) in view of Enoki, "Delay Time Analysis for 0.4- to 5-micron-Gate InAlAs-InGaAs HEMT," (Enoki).

a. Sawada discloses a Doped Channel – Heterojunction Field Effect Transistor (DC-HFET) having a doped channel composed of n-InGaAs; a doped barrier (or semiconductor structure) composed of n-AlGaAs (a material having a lower electron-affinity than that of the channel); and a doped contact composed of n-GaAs. An ohmic electrode is formed on the GaAs

Art Unit: 2815

contact layer and a Schottky electrode is formed on the barrier layer semiconductor structure. To clarify the record for appeal, a “heterojunction” is a junction formed by layers of two dissimilar materials (e.g., between InGaAs and AlGaAs), regardless of whether either of these two layers is doped with impurities (e.g., n-type or p-type impurities) or undoped (e.g., intrinsic or i-AlGaAs). An “isotype” junction is a junction between two layers that are both doped with the same type of doping impurities (e.g., both layers are either n-doped or p-doped). These definitions are not in dispute. The doped AlGaAs barrier forms isotype heterojunctions with the InGaAs channel and the GaAs contact layers. Sawada further teaches that various structural- and doping-configuration modifications for the barrier layer may be employed with the DC-HFET to further optimize or adjust various conventionally-understood device parameters. For example, compare the embodiment of FIG 1 wherein an undoped barrier exists between the n-doped InGaAs channel and the n-GaAs cap with the embodiment of FIG 6 wherein the barrier layer is undoped beneath the gate and doped beneath the source and drain, thereby maintaining an enhanced gate Schottky barrier while reducing the series resistance between the channel and the cap layers (page 355, col. 1, section 4, first paragraph).

Sawada does not anticipate the claims because it does not teach the further inclusion of an undoped layer/region disposed between the doped top and the bottom regions of the AlGaAs barrier layer, nor that the gate makes Schottky contact particularly to this undoped layer region (claim 14).

b. Enoki teaches periodic table group-III-As (or As-based) high electron mobility transistor (HEMT) HFETs that comprise an n-InGaAs channel; an InAlAs “semiconductor structure” comprised successively of an n-doped, undoped, and n-doped layer; an n⁺ InGaAs

Art Unit: 2815

contact layer for connection of ohmic electrodes; and a Schottky gate that contacts the middle, undoped layer of the "semiconductor structure." (See e.g., FIG 1) Enoki specifically states that "the undoped InAlAs layer between two highly doped InAlAs layers is to enhance the Schottky barrier of the gate metal. The upper n⁺-InAlAs layer is designed to reduce the source and drain series resistance." (Page 502, col. 1, section II)

c. It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified the Sawada n-AlGaAs barrier layer by providing an additional undoped layer between the top and bottom portions (or restated, by temporarily stopping and restarting the n-type impurity dopant supply during the growth of the barrier layer) for the purpose of enhancing the Schottky barrier of the gate while simultaneously providing a source/drain series resistance that is reduced relative to if the upper portion of the barrier was undoped, as taught by Enoki; and also for the purpose of providing both of these advantages while simultaneously obviating the need for the additional masking steps that would be required to achieve the structure of Sawada's FIG. 6 embodiment wherein the dopant implant is provided for only the S/D regions.

d. Regarding claims 3, 5 and 7, while Sawada discloses a DC-HFET having a heavily doped channel, barrier and cap layer, wherein the respective junctions are all iso-type heterojunctions, Sawada does not teach the limitations of claim 3 which recites that the layers of the channel/barrier junction and the barrier/contact junction are all doped 1E18. Rather, Sawada--while also disclosing that these layers are all heavily doped to the same order of magnitude--sets forth specific, slightly higher doping concentrations for the channel, barrier and contact layers of 2.5E18, 1.5E18 and 3E18, respectively.

Nonetheless, it would have been obvious to one of ordinary skill in the art at the time of the invention to have modified the doping concentrations to the particular doping levels set forth in claim 3 because the doping levels of the Sawada layers are all heavily doped to the same order of magnitude as that claimed, and such minor changes to the doping levels would not produce any unexpected results, but rather constitute an optimization of results readily obtainable through routine experimentation: more specifically, lowering the barrier doping concentration from 1.5×10^{18} to 1×10^{18} would merely produce the expected results of proportionally increasing the gate-barrier layer Schottky barrier and slightly increasing the source/drain resistance; decreasing the channel doping from 3×10^{18} to 1×10^{18} would slightly reduce both the channel/barrier heterojunction barrier and the carrier-impurity scattering in the channel; and reducing the contact doping from 3×10^{18} to 1×10^{18} would proportionally increase the source and drain resistances.

(10) Response to Argument

Claims 1 – 10 and 12 – 15 are properly rejected under 35 U.S.C. §103(a) as being unpatentable over Sawada in view of Enoki.

Introduction:

Semiconductor compounds such as GaAs, AlGaAs, InGaAs, InAlAs, etc., are conventional. When a given semiconductor, such as AlGaAs, for example, is effectively devoid of impurity dopants (or more simply, “impurities” or “dopants”), it is conventionally called either an “undoped” or “intrinsic” semiconductor, and is conventionally notated with either of the following synonyms: “u-AlGaAs” or “i-AlGaAs.” Alternatively, if the AlGaAs is doped with certain impurities known as “n-type impurities,” it is called, “n-doped AlGaAs” or more simply, “n-AlGaAs.” Two adjacent layers having the same base composition but different

Art Unit: 2815

doping concentrations (e.g., n-AlGaAs and i-AlGaAs) are said to form a "homojunction." This background terminology is not disputed.

HFETs are conventional, and it was known that they may be made from various semiconductor material systems. Typically, HFETs generally include a substrate; a buffer layer overlying the substrate that improves the subsequently-grown layers' crystallinity; a relatively-small bandgap channel layer formed on the buffer; at least one relatively-large bandgap barrier layer overlying the channel; and a source/drain (S/D) ohmic contact layer overlying the barrier layer. It was generally known that various modifications could be made to one or more of these layers. None of this is disputed.

The prior-art reference, Sawada, discloses an HFET that is composed of layers of Group III-As semiconductor materials selected so that that the HFET can be formed on a GaAs substrate (i.e., from the bottom up: a GaAs substrate; a GaAs buffer; an InGaAs channel; an AlGaAs barrier; and a GaAs S/D contact layer). Sawada's barrier layer is specifically composed of a single layer of n-AlGaAs. The prior-art reference, Enoki, discloses an HFET that is composed of layers of Group III-As semiconductor materials selected so that that the HFET can be formed on an InP substrate (i.e., from the bottom up: an InP substrate; an InAlAs buffer, an InGaAs channel, plural InAlAs layers, and an InGaAs S/D contact layer). Enoki's barrier layer is specifically composed of three consecutive layers of n-InAlAs / i-InAlAs / n-InAlAs, or an "n-i-n homojunction barrier layer scheme." Underneath the n-i-n homojunction barrier, Enoki also includes an additional 20-angstrom i-InAlAs barrier spacer layer that separates the lower n-InAlAs barrier layer from the InGaAs channel. None of this is disputed.

The Examiner's rejections are based upon converting Sawada's single-layer, n-AlGaAs barrier into a three-layer barrier wherein the lower and upper sub-layers are still composed of n-AlGaAs, but wherein the middle AlGaAs layer/region is instead composed of i-AlGaAs: that is, forming the barrier as three consecutive layers of n-AlGaAs / i-AlGaAs / n-AlGaAs, or an "n-i-n homojunction barrier layer scheme." More specifically, the Examiner's position is that (1) modifying Sawada's HFET—by substituting a three-layer, n-i-n homojunction, AlGaAs barrier for the disclosed single-layer n-AlGaAs barrier layer—will result in the claimed HFET device; (2) Enoki teaches this specific n-i-n homojunction HFET barrier layer scheme (albeit in an InAlAs barrier instead of an AlGaAs barrier); and (3) Enoki also provides motivation for why the skilled artisan would have wanted to employ such an n-i-n homojunction barrier layer scheme in other HFETs, such as Sawada's HFET.

Appellant has not disputed that combining Sawada and Enoki in the manner set forth by the rejection (hereinafter, "the Sawada/Enoki HFET" or "the combination") would produce every structural element claimed. Appellant has not disputed that the Sawada/Enoki HFET would generally function in the same manner as the present invention. Appellant has not disputed that the Sawada/Enoki barrier would specifically produce the same beneficial bandgap phenomenon as the present invention. Appellant has not disputed that actually making the Sawada/Enoki HFET (e.g., by temporarily stopping the n-dopant impurity source during the barrier-layer growth process) was well within the capability of the reasonably skilled artisan at the time of the invention. Because these issues are not disputed, they are treated as admitted by the Appellant.

The only issue on appeal is whether sufficient motivation existed to combine Sawada and Enoki in the manner that admittedly does produce the claim invention as claimed and disclosed.

Art Unit: 2815

The Examiner's rejection set forth fully proper and adequate motivation to combine Sawada and Enoki, thereby establishing a prima facie case of obviousness. As such, the burden has shifted to Appellant to rebut this prima facie showing obviousness. All of Appellant's arguments on appeal are without merit. As such, Appellant has failed to rebut the Examiner's prima facie showing of obviousness.

Each of Appellant's arguments is now addressed in the order raised:

First:

With regard to appellant's argument that "Enoki et al. teach that the highly doped n+-InAlAs layer, not, as alleged by the Examiner, the undoped i-InAlAs layer, is used to reduce the source and drain series resistance," it should be noted that the entire n-i-n barrier layer of Enoki provides benefits when used in the invention of Sawada. In this case the intermediate undoped layer between the doped layers is used "for the purpose of enhancing the Schottky barrier of the gate while" the doped n+-InAlAs upper layer remains in contact with the "n+-InGaAs" source/drain contact layer in Enoki thus "simultaneously providing a source/drain series resistance that is reduced relative to if the upper portion of the barrier was undoped." [See paragraph c. on page 3 of the outstanding Office Action, repeated above. Emphasis added]. Appellant is arguing a feature of the n-i-n barrier layer that is not being attributed to the undoped "i-InAlAs layer" in the rejection, rather this feature is credited to the upper doped n+-InAlAs layer of the n-i-n barrier layer as stated in Enoki and relied upon in the rejection. Therefore, appellant's arguments are not persuasive and the rejection is proper.

Art Unit: 2815

With regard to appellant's argument that "...admitted to by the Examiner in the last paragraph on page 7 of the outstanding Office Action, the addition of the undoped layer to the device in Fig. 1 of Sawada et al. would increase the resistance," it should be noted that this statement misconstrues the Examiner's position set forth on page seven of the outstanding Office Action. The point made by the Examiner is that "Enoki also teaches that the further inclusion of the upper highly n-doped barrier layer reduces the series resistance, at least sufficiently to allow the HFET to operate as intended. As such, the further inclusion of an undoped layer composed of the same material as the rest of Sawada's barrier layer would not cause the barrier to possess unsatisfactorily high resistance. This is because the additional presence of the upper, highly n-doped region of the AlGaAs barrier layer that forms a junction with the GaAs source-drain (S/D) contact layers in Sawada would sufficiently reduce the S/D series resistance to allow the Sawada HFET to operate as intended, as taught by Enoki." [See last paragraph on page 7 of the outstanding Office Action, repeated above. Emphasis added]. The combination does not substitute an undoped barrier for a doped barrier. Rather, The combination includes the undoped barrier layer of Enoki in Sawada only with the inclusion of both the top and bottom highly doped barrier layers. By including in Sawada all three of the barrier layers of Enoki's n-i-n homojunction barrier layer scheme the series resistance is not unduly increased, as would be the case if the combination only included the undoped barrier layer of Enoki in Sawada. Therefore, appellant's arguments are not persuasive and the rejection is proper.

Second:

With regard to appellant's argument that "Applicant's do not understand the Examiner's reference to Fig. 6 of Sawada et al. as it is directed to a different embodiment that clearly has a much different structure than the embodiment shown in Fig. 1 of Sawada et al.," it should be noted that that appellant's failure to understand the Examiner's cogent rejection is not a legally-recognized basis for rebutting an obviousness rejection. The reference to figure 6 of Sawada provides additional motivation for including the doped barrier layers and the undoped barrier layer of Enoki as the barrier layer in the figure 1 embodiment of Sawada. In figure 6 of Sawada, and the supporting description on page 355, section 4, first paragraph, motivation for having an undoped barrier is given. In this embodiment of Sawada, an undoped barrier layer is used to have a high Schottky barrier between the gate and channel. Further, figure 6 of Sawada uses a different scheme than the combination to reduce the series resistance between the channel and the source/drain contacts. Namely, this alternative embodiment of Sawada uses an implantation technique, instead of the multiple layer technique of the combination. Sawada's figure 6 reinforces the combination in that it further proves that the highly doped barrier layers of Enoki must be employed in Sawada, figure 1, when using the undoped barrier layer of Enoki in the combination, so that the resistance is reduced in the source drain regions. Therefore, appellant's arguments are not persuasive and the rejection is proper.

With regard to appellant's argument that "Fig. 6 of Sawada et al. clearly fails to teach or suggest, at least, a contact layer," it should be noted that Sawada, figure 6, is not relied upon for the combination of the rejection, but merely as supporting evidence. The combination primarily relies on the embodiment of figure 1 in Sawada in combination with figure 1 of Enoki. Therefore, appellant's arguments are not persuasive and the rejection is proper.

Third:

With regard to appellant's argument that: "...the Examiner has failed to provide any evidence that one of ordinary skill in the art at the time of the Applicant's invention would have expected the effect of enhancing the Schottky barrier could be achieved by providing an undoped AlGaAs layer in between two doped AlGaAs layers. Enoki et al. fails to teach or suggest that the effect of enhancing the Schottky barrier produced by providing an undoped InAlAs layer between two highly doped InAlAs layers would be produced in an undoped AlGaAs layer were provided between two doped AlGaAs layers," it should be noted that physics principles of III-V semiconductors are consistent across the different types of III-V materials. As explained in the paragraph bridging pages 6 and 7 of the Office Action dated May 18, 2004, one of ordinary skill would recognize that the benefit of having an undoped barrier layer of InAlAs sandwiched by two highly doped barrier layers of InAlAs would also apply to a device wherein the barrier layers were made of AlGaAs. Both InAlAs and AlGaAs are commonly used III-V semiconductor materials. One of ordinary skill in the art would recognize that a barrier layer consisting of undoped AlGaAs sandwiched by highly doped layers of AlGaAs would provide the same benefits as an undoped barrier layer of InAlAs sandwiched by two highly doped barrier layers of InAlAs, in their respective devices, because they are both III-V semiconductor barrier materials. Applicant has not provided any evidence that the relevant physical properties of barrier layer consisting of undoped AlGaAs sandwiched by highly doped layers of AlGaAs would be qualitatively or unexpectedly different than an undoped barrier layer of InAlAs sandwiched by

Art Unit: 2815

two highly doped barrier layers of InAlAs. Therefore, appellant's arguments are not persuasive and the rejection is proper.

In response to appellant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., barrier layers of AlGaAs would not provide the same benefits as barrier layers of InAlAs) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). In this case, the claims do not recite any specific III-V material. Therefore, appellant's arguments are not persuasive and the rejection is proper.

Appellant's third set of arguments are somewhat related to his fifth set of arguments. Thus the above arguments are addressed further in the fifth section, infra.

Fourth:

With regard to appellant's argument that "by the Examiner's reasoning, the device in Fig. 1 of Sawada et al. would have a higher Schottky barrier than the device in Fig. 1 of Enoki et al. because the barrier layer of the device in Fig. 1 of Sawada et al. has less than half of the n-doping of the barrier layer of the device in Fig. 1 of Enoki et al.," it should be noted that this is not an accurate portrayal of the facts of the combination. First, a higher Schottky barrier is desired between the barrier layer and the gate (page 502, col. 1, section II of Enoki). Second, "...the more heavily n-doped a barrier layer is... the lower the gate Schottky barrier is." Likewise, the opposite is true: the lower the barrier's doping level is, the higher the gate Schottky barrier is. These facts relate to the contact area directly between the gate and the barrier. The barrier/gate contact in Sawada, figure 1, has a lower Schottky barrier than the barrier/gate contact of Enoki,

Art Unit: 2815

figure 1, because the gate (T-shaped shaded structure) of Sawada contacts a doped barrier (n-AlGaAs), while the gate (Gate Ti/Au) of Enoki contacts an undoped barrier (i-InAlAs). Thus, one of ordinary skill in the art would conclude that there is sufficient motivation for combining the n-i-n barrier layer scheme of Enoki with Sawada because the undoped (less doped) barrier/gate contact provides a higher Schottky barrier than the doped barrier/gate contact of Sawada. Further, the highly doped barrier layers sandwiching the undoped barrier layer of Enoki, which do not directly contact the gate, provide for decreased source/drain resistance as outlined in the combination. Therefore, appellant's arguments are not persuasive and the rejection is proper.

With regard to appellant's argument that "Examiner has failed to explain why one of ordinary skill in the art at the time of the Applicants' invention would have desired to further enhance the Schottky barrier of the barrier layer of the device in Fig. 1 of Sawada et al.," it should be noted that it is sufficient that Enoki teaches a barrier layer which provides enhanced properties for the Schottky gate and reduced source/drain contact resistance (page 502, col. 1, section II of Enoki). One of ordinary skill would recognize that enhancing the Schottky gate while simultaneously decreasing series resistance in the source drain regions is desirable in the device of Sawada based on the teaching of Enoki. The burden is on the appellant to prove that the motivation fails. The appellant has not provided any evidence that the barrier layer of Enoki would not benefit the device of Sawada. Therefore, appellant's arguments are not persuasive and the rejection is proper.

Fifth:

With regard to appellant's argument that "contrary to the Examiner's allegation, Enoki et al. does not teach this... The examiner has failed to explain how this very specific teaching of Enoki et al. substantiates his much broader allegations;" it should be noted that a reference should not be read too narrowly such that only the embodiment disclosed is the only teaching that can be gleaned therefrom. An example that one of ordinary skill in the art would impress the teaching of Enoki on a broader concept of III-V semiconductor devices can be found in figures 2 and 13, with the supporting text thereof, of United States Patent number 5,404,032 (made of record in the PTO-892 filed December 5, 2001, see appendix A attached hereto). These figures clearly show HEMT structures based on both AlGaAs-GaAs (figure 2, with a AlGaAs barrier layer) and InP (figure 13, with a InAlAs barrier layer) systems. It is noted that Enoki teaches an In-P based HEMT (see the introduction, section I of Enoki, page 502) and that Sawada teaches an AlGaAs-GaAs based HEMT (see the first line of the abstract of Sawada). Thus, one of ordinary skill in the art, when considering such known art as the '032 reference, would recognize that Enoki's teachings—of a three-layer, n-i-n homojunction barrier structure scheme and it's benefits over a single n-layer barrier structure scheme—have general applicability to HFET barriers composed of various conventional Group III-V material systems, even though Enoki provides an example of only one particular III-V material system. Namely "that including an undoped layer between sandwiching heavily doped barrier layers and in contact with the gate metal will increase the gate Schottky barrier relative to if the undoped layer was not present, at least when (1) the undoped layer is composed of the same base composition as the doped barrier layers (i.e., the doped/undoped/doped barrier layers form two homojunctions); and (2) the doped barrier layers are n-doped on the order of 10^{18} (i.e., at least

Art Unit: 2815

a few orders of magnitude greater than the undoped layer.” Appellant has not provided any proof that this broader concept is not true. The mere fact that Enoki teaches that this broader concept is true for the disclosed n^+ -InAlAs/I-InAlAs/ n^+ -InAlAs barrier layer in an In-P based InAlAs-InGaAs HEMT is enough teaching for one of ordinary skill to recognize that it would be true for an AlGaAs barrier layer of the AlGaAs-GaAs based HEMT of Sawada arranged in the same doped/undoped/doped fashion. Further, the claims are not directed to a specific III-V layer, but instead are directed to a generic III-V HEMT. Both Sawada and Enoki teach III-V HEMT's, and thus one of ordinary skill would have recognized that the claimed barrier layer structure scheme that is beneficial for Enoki would also be effective for Sawada based on the broader teaching of Enoki. Therefore, appellant's arguments are not persuasive and the rejection is proper.

With regard to appellant's argument that “Examiner has failed to provide any evidence to substantiate...” the “...allegation...” that “...this effect also applies to semiconductor material systems other than InAlAs is based on the well-understood physics principles that in an undoped III-V semiconductor, the Fermi energy level is positioned approximately midway between the conduction and valence band, and that n-doping III-V semiconductor materials shifts the Fermi energy level towards the conduction band,” it should be noted that the burden has shifted to the appellant to prove that this is not well known and a physical property of III-V semiconductor materials. As above, reading Enoki too narrowly does not reflect the knowledge one of ordinary skill in the art would glean therefrom when evaluating the III-V HEMT's of Sawada and Enoki. As an aside, it is noteworthy that Appellant has not provided any evidence refuting this allegation. In fact, Appellant has not even alleged that this allegation is in any way inaccurate.

Art Unit: 2815

Appellant only argues that the examiner has failed to provide any evidence to support this allegation. The problem with Appellant's argument is threefold. First, Appellant had never requested that such evidence be provided during prosecution. Because it was first raised on appeal, Appellant's request for further evidence is untimely. Second, various references of record (e.g., Sawada USPAT 5,404,032) do substantiate this allegation. Third, Appellant is not arguing that the Examiner failed to provide a basis for the reasonable expectation of success. Rather, Appellant implicitly acknowledges that the Examiner provided a basis for the reasonable expectation of success, and thereby did what was legally required to establish a prima facie case of obviousness. But Appellant is arguing that the Examiner has failed to provide evidence to support the technical veracity of the reasons that provide the basis for the reasonable expectation of success. Appellant has cited no authority for the proposition that establishment of a prima facie case of obviousness requires the Examiner meet this additional burden. Restated, the Examiner has already established a prima facie case of obviousness. The burden has shifted to Appellant to rebut the prima facie case of obviousness. Appellant's argument—that the Examiner did not provide all of the tertiary evidence that the Appellant untimely requested—is not an allegation that the examiner's motivation to combine the prior art references was improper. It is not evidence that the Examiner's basis in support of a reasonable expectation of success was either inadequate or inaccurate. And the argument therefore does not rebut the prima facie case that was already established by the Examiner. Therefore, Appellant's arguments are not persuasive, and the rejection is proper.

MPEP 2143.02 states, "Obviousness requires only a reasonable expectation of success."

In this case it would have been obvious to incorporate the III-V, n-i-n homojunction barrier layer

Art Unit: 2815

scheme of Enoki into the barrier layer of Sawada's III-V HFET in order to enhance the gate Schottky barrier and simultaneously reduce the series resistance of the source/drain region as taught by Enoki. The n-AlGaAs barrier layer of Sawada may be modified to the n-i-n barrier layer scheme of the InAlAs layers of Enoki in view of the fact that one of ordinary skill (see figures 2 and 13 of the '032 reference) would recognize that the aforementioned III-V semiconductor barrier layers would be expected to have similar physical properties because the chemical difference between the III-V compounds involves known elemental replacements (i.e. "InAlAs" for "AlGaAs") and because physics principles are known to be similar across III-V semiconductor layers. Therefore, appellant's arguments are not persuasive and the rejection is proper.

Sixth:

With regard to appellant's argument that "Examiner has failed to provide any evidence to support..." the "...allegation" "in the last paragraph on page 7," it should be noted that Enoki has clearly been cited as evidence to teach "these allegations." As recited in the rejection, repeated above, Enoki teaches page 502, column 1, first paragraph under section II "The undoped InAlAs layer between two highly doped InAlAs layers is to enhance the Schottky barrier of the gate metal. The upper n⁺-InAlAs layer is designed to reduce the source and drain series resistance." Therefore, appellant's arguments are not persuasive and the rejection is proper.

With regard to appellant's argument that "Even if the Examiner's allegation that the effect of the junction between the n-doped AlGaAs barrier layer and the n-doped GaAs contact

Art Unit: 2815

layer is to lower the resistance is true, that effect would be present before modifying the device of Fig. 1 of Sawada et al. to have an undoped layer," it should be noted that there are two reasons to use the doped-undoped-doped barrier layer of Enoki in the device of Sawada. While the device in figure 1 of Sawada, unmodified, does have low resistance in the source/drain contact area, the Schottky gate is not improved. When using the barrier layer of Enoki in the device of Sawada, as combined, both the Schottky barrier is enhanced and the resistance in the source/drain region is reduced. Therefore, appellant's arguments are not persuasive and the rejection is proper.

With regard to appellant's argument that "the effect of adding an undoped layer to the device of Fig. 1 of Sawada et al. is to increase the resistance," it should be noted that this is not in line with the complete combination of using the doped-undoped-doped barrier layer scheme of Enoki in the device of Sawada. The argument that the combination would "increase the resistance" in the source/drain regions of the Sawada reference would be true only if an undoped barrier was used alone instead of the doped-undoped-doped barrier of the combination. When the combination is considered as a whole, and the entire doped-undoped-doped barrier scheme of Enoki is combined as the barrier layer of Sawada, one of ordinary skill would recognize that both the Schottky barrier is enhanced and the resistance in the source/drain region is reduced. Therefore, appellant's arguments are not persuasive and the rejection is proper.

With regard to appellant's argument that "the Examiner has failed to provide any evidence that one of ordinary skill in the art would have considered the modified device of Fig. 1 of Sawada et al. having a higher resistance to be satisfactory," it should be noted that the modified device of figure 1 of Sawada and Enoki does not have higher resistance in the

Art Unit: 2815

source/drain regions. Thus, no evidence needs to be provided that a higher resistance in the source/drain region of Sawada is satisfactory. Instead, it is clear that a higher resistance in the source/drain region is not satisfactory because the combination clearly has a reduced resistance in the source/drain regions. It is maintained that when the combination is considered as a whole, and the entire doped-undoped-doped barrier scheme of Enoki is combined as the barrier layer of Sawada, one of ordinary skill would recognize that both the gate Schottky barrier is enhanced and the resistance in the source/drain region is reduced. Therefore, appellant's arguments are not persuasive and the rejection is proper.

With regard to appellants argument that "Sawada et al. clearly teaches, as acknowledged by the Examiner, that it is desirous to have a reduced resistance in the discussion of the 'new device structure' in Fig. 6," it should be noted that the combination does have a reduced resistance in the source/drain region. Sawada's figure 6, and supporting text, is used merely as evidence to support the fact that when using the doped/undoped/doped barrier scheme of Enoki in the device of Sawada, figure 1, the upper-doped barrier layer is necessary in the combination in order to maintain reduced resistance in the source/drain region. When the combination is considered as a whole, and the entire doped-undoped-doped barrier scheme of Enoki is combined as the barrier layer of Sawada, one of ordinary skill would recognize that both the Schottky barrier is enhanced and the resistance in the source/drain region is reduced. Therefore, appellant's arguments are not persuasive and the rejection is proper.

Claims 1 – 10 and 12 – 15 are unpatentable over Sawada et al. and Enoki et al.


Art Unit: 2815

In conclusion, it is noted that MPEP 2143.02 states, "Obviousness requires only a reasonable expectation of success." In this case it would have been obvious to use the III-V, doped-undoped-doped barrier layer scheme of Enoki as a barrier layer in the device of Sawada in order to enhance the Schottky barrier and simultaneously reduce the series resistance of the source/drain region as taught by Enoki. Clearly this motivation provides a reasonable expectation of success for the combination. Therefore, appellant's arguments are not persuasive and the rejection is proper.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,


Paul E Brock II



PAUL E. BROCK II
PRIMARY EXAMINER

Conferees:

B. William Baumeister



B. WILLIAM BAUMEISTER
SUPERVISORY PATENT EXAMINER

Tom Thomas



Olik Chaudhuri

